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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,450	04/24/2002	Yoshiyuki Ando	YA02	6566

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EXAMINER	
MILLER, CRAIG S	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10/063,450	Yoshiyuki
Examiner	**Group Art Unit**
Craig Steven Miller	2857

—Th MAILING DATE of this communication appears on th cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 12/17/03.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-25 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-25 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ Th drawing(s) filed on _____ is/are objected to by the Examiner

☐ Th specification is objected to by the Examiner.

☐ Th oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)–(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)–(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Atta hment(s)

☐ Inf rmation Disclosure Stat ment(s), PTO–1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO–892

☐ Notice of Draftsperson's Pat nt Drawing R view, PTO–948

☐ Int rview Summary, PTO–413

☐ Notice of Informal Patent Application, PTO–152

☐ Oth r _____

Office Acti n Summary

1. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*
>
> *Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.*

4. Claims 1, 2 and 4-25 are rejected under 35 U.S.C. 103 as being unpatentable over Sugawara (5,781,060) in view of Stapleton *et al.* (6,574,577 B2).

As to claims 1, 2, 4-6, 8-10 and 15-25, Sugawara discloses test an IC to determine appropriate operating voltages (col. 4 lines 30+), and to control the voltage as a function of internal (col. 3 lines 26+) control signals from registers (col. 3). Sugawara neither discloses that the desired voltage values are stored within tables nor specifies that the desired voltages should be determined at various clock speeds. Stapleton *et al.* discloses the processor sending a desired voltage level to a voltage regulator to control desired core voltage supply (fig. 1 and abstract) and that this desired voltage should be determined after fabrication (col. 1 lines 49+). Reference data tables are a well known method of internally storing data for future uses within the IC art. Because the devices of Sugawara and Stapleton *et al.* are within the art of circuit supply voltage, because Stapleton *et al.* discloses that the desired values should be internally stored and because reference data tables are a well known method of storing such data, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara internal stored desired voltage data within reference data tables so as to receive the expected benefits derived there from such as enhanced system flexibility absent a showing of unexpected results or synergistic results from any particular claimed combination.

More particularly with respect to claims 6, 7, 24 and 25, said claims are directed towards determining conventional ranges of operation of processor voltages and clock speeds. The

Examiner notes In re Aller, 105 USPQ 233 (CCPA 1955), "*...changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art.*" In re Dreyfus, 22 CCPA (Patents) 830, 73 F.2d 931, 24 USPQ 52 and In re Waite et al., 35 CCPA (Patents) 1117, 168 F.2d 104, 77 USPQ 586.

More particularly with respect to claims 8-10, said claims are directed towards well known IC testing design parameters. Because the device of Sugawara as modified above is in the art of IC testing and because it is known to perform testing using such test design criteria, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above such known testing criteria so as to receive the expected benefits derived there from such as enhanced system reliability absent a showing of unexpected results or synergistic results from any particular claimed combination.

More particularly with respect to claim 11, said claim is directed towards well known IC testing during manufacturing. Because the device of Sugawara as modified above is in the art of IC testing and because it is known to perform testing during the manufacturing process, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above such known manufacturing testing so as to receive the expected benefits derived there from such as enhanced system reliability absent a showing of unexpected results or synergistic results from any particular claimed combination.

As to claims 12 and 13, said claims are directed towards storing plural known voltages or operating value of interest in IC operation. Sugawara as modified above discloses control of circuit supply voltages in general but does not specify that several voltages should be controlled. The Examiner notes that it is well known to use multiple means for multiple effect, St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). It is also known that ICs commonly have plural supply voltages of interest. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above the controlling of several known supply voltages so as to receive the expected

benefits derived there from such as enhanced system reliability absent a showing of unexpected results or synergistic results from any particular claimed combination.

More particularly with respect to claims 13, 24 and 25, said claims are directed towards ensuring proper IC operation at plural clock speeds of interest. Sugawara as modified above discloses control of circuit supply voltages in general but does not specify that the testing should be performed at several clock speeds of interest. The Examiner notes that it is well known to use multiple means for multiple effect, St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). It is also known that ICs commonly have plural clock speeds of interest and that IC tests are commonly tested at ever increasing plural clock speeds during IC testing. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above the IC testing at several known clock speeds of interest so as to receive the expected benefits derived there from such as enhanced system reliability absent a showing of unexpected results or synergistic results from any particular claimed combination.

As to claim 14, said claim is directed towards well known IC testing design parameters. Because the device of Sugawara as modified above is in the art of IC testing and because it is known to perform testing using such test design criteria, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above such known testing criteria so as to receive the expected benefits derived there from such as enhanced system reliability absent a showing of unexpected results or synergistic results from any particular claimed combination.

More particularly with respect to claims 15, 16, 24 and 25, said claims are directed towards the IC performance improvement being defined as improved clock speeds or operating voltage ranges. Because the device of Sugawara as modified above is in the art of IC testing and because it is known to perform testing using such test design criteria goals, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above such known testing goals so as to receive the expected benefits derived there from such as enhanced system reliability at improved clock speeds or

increased operating voltage ranges absent a showing of unexpected results or synergistic results from any particular claimed combination.

3. Claim 3 is rejected under 35 U.S.C. 103 as being unpatentable over Sugawara in view of Stapleton *et al.* as applied to claims 1 and 2 above and further in view of Cantone *et al.* (6,675,360 B1).

Claim 3 is directed towards using an anti-fuse method to store the internal reference data. Cantone *et al.* discloses that fuse burning should be used to store reference data within an IC. Because the devices of Sugawara, Stapleton *et al.* and Cantone *et al.* are within the art of circuit voltage supply and because Cantone *et al.* discloses that fuse burning is a known method to internally store data, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Sugawara as modified above, the internal stored desired voltage data being fuse burned within reference data tables so as to receive the obvious benefits derived there from such as enhanced data integrity absent a showing of unexpected results or synergistic results from any particular claimed combination.

4. The prior art made of record but not relied upon is deemed pertinent to applicant's disclosure.

Mittal *et al.* (5,719,800) discloses performance throttling to reduce IC power consumption.
Gupta *et al.* (5,996,083) discloses an IC with programmable power consumption.
Sandhu *et al.* (6,006,169) discloses trimming an IC.
Manning (6,320,453 B1) discloses lowering IC standby current.
Bertin *et al.* (6,345,362 B1) discloses managing reduced power using a status table.

5. No IDS form was found within the paper record but applicant's discription of the art filed within said IDS was found and said prior art is listed within the attached PTO-892. Any inconvenience is regretted, no further action is required by the Applicant on this issue.

5. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Craig Steven Miller whose telephone number is (571) 272-2219. Central facsimile services are now available at (703) 872-9306.

The Examiner can normally be reached on Mondays through Fridays from 7:30am-4:00pm EST. Should repeated attempts to reach the Examiner be unsuccessful, the Examiner's Supervisor, Marc Hoff may be reached at (571) 272-2216.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Craig Steven Miller (ss)
09 January 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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